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CANCEL CLAIMS 1-33 AND 41-144

34. In combination for use in a system providing signals having individual ones of a plurality of analog levels to represent information and including a hub and a computer displaced from the hub and including a plurality of twisted pairs of wires extending between the hub and the computer, one of the twisted pairs of wires providing only for the transmission of the signals from the computer to the hub, a second one of the twisted pairs of wires providing only for the reception at the computer of the signals from the hub, third and fourth ones of the twisted pairs of wires selectively providing for the transmission of the signals from the computer to the hub and the reception at the computer of the signals from the hub,

first means responsive at the computer to the signals received at the second, third and fourth ones of the twisted pairs for providing a digital conversion of such signals at a particular value of frequency,

timing recovery means responsive at the computer to the digital conversions from the first means for regulating at the particular value the frequency of the digital conversions by the first means, and

digital adaptive equalizer means responsive at the computer to the signals from the first means for selecting individual ones of the analog levels closest in magnitude to the digital conversions from the first means.

35. In a combination as set forth in claim 34,

second means responsive at the computer to the received signals for providing an automatic gain control of such signals and for introducing such signals to the first means, and

third means responsive at the computer to the digital conversions from the first means for regulating the gain of the signals from the second means at a particular value,

the digital adaptive equalizer means being responsive to the digital conversions from the first means for selecting the individual ones of the analog levels closest in magnitude to the digital conversions from the first means.

36. In a combination as set forth in claim 34,

second means responsive at the computer to the signals from the digital adaptive equalizer means for recovering the information represented by the analog levels selected by the digital adaptive equalizer means.

37. In a combination as set forth in claim 34,

the received signals being in the form of packets each including a plurality of timing signals in a preamble at the beginning of such packet and including data signals after the preamble, and

the timing recovery means including second means responsive to the timing signals in each packet for regulating at the particular value the frequency at which the first means provides a digital conversion of the signals received at the computer.

38. In a combination as set forth in claim 34,

the received signals being in the form of packets each including a plurality of timing signals at the beginning of such packet and including data signals after the preamble,

the timing recovery means including second means responsive to the timing signals in each packet for regulating at the particular value the frequency at which the first means provides the digital conversion of the data signals received at the computer in each packet, and

third means responsive to the analog levels selected by the digital adaptive equalizer means for the data signals in each packet for recovering the data represented by such selected analog levels.

39. In a combination as set forth in claim 35,

the received signals being in the form of packets each including a plurality of timing signals at the beginning

of such packet and including data signals after the preamble,

the timing recovery means including fourth means responsive to the timing signals in each packet for regulating at the particular value the frequency at which the first means provides a digital conversion of the signals received at the computer in each packet, and

fifth means responsive to the analog levels selected by the digital adaptive equalizer means in each packet for recovering the data represented by such selected analog levels.

40. In a combination as set forth in claim 38,

fifth means disposed at the computer for regulating at the particular value, in accordance with the pattern of successive ones of the signals in each packet, the frequency at which the first means provides a digital conversion of the signals received at the computer.

Add the following new claims:

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-- 145. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal, comprising:

an analog to digital converter for digitally converting the multi-level signal at a particular rate;

a timing recovery circuit for regulating the particular rate at which said analog to digital converter converts the multi-level signal; and,

a digital adaptive equalizer for receiving the digitally converted multi-level signal and selecting one of a plurality of levels. --

-- 146. The apparatus of claim 145, further comprising an automatic gain control circuit coupled to said analog to digital converter. --

-- 147. The apparatus of claim 145, further comprising a decoder circuit coupled to said digital adaptive equalizer. --

-- 148. The apparatus of claim 147, further comprising a media access controller coupled to said decoder circuit. --

-- 149. The apparatus of claim 145, wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer. --

-- 150. The apparatus of claim 145, wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of peak signal samples. --

-- 151. An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal transmitted at a transmission rate of at least 25 megasymbols per second, comprising:

an analog to digital converter that is responsive to the multi-level signal transmitted at the transmission rate of at least 25 megasymbols per second;

a clock recovery circuit coupled to said analog to digital converter; and,

a digital adaptive equalizer coupled to said analog to digital converter. --

Kindly cancel claims 152-162.

163. (Amended) A method for recovering a plurality of analog levels defining information signals transmitted on at least one pair of twisted wires comprising:

converting the plurality of analog levels defining information signals to corresponding digital information signals at a particular rate;

regulating the particular rate of conversion; and

identifying one of the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

164. (Amended) The method of claim 163, wherein the particular rate is regulated in accordance with a product of a plurality of signal samples.

-- 165. The method of claim 163, wherein the particular rate is at least 25 megasymbols per second. --

166. (Amended) The method of claim 163, and further comprising decoding the identified digital information signal.

Kindly add new claims 167-213 as follows:

167. (New) An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a plurality of analog levels defining information signals, comprising:

a clock arranged to generate clock signals having a phase;

an analog to digital converter arranged to convert the plurality of analog levels to corresponding information digital signals in response to the clock signals;

a timing recovery circuit arranged to shift the phase of the clock signals so that the time at which the analog to digital converter samples the analog levels is adjusted; and

a digital adaptive equalizer arranged to receive the digital information signals and to identify one of the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

168. (New) The apparatus of claim 167, further comprising an automatic gain control circuit coupled to said analog to digital converter.

169. (New) The apparatus of claim 167, further comprising a decoder circuit coupled to said digital adaptive equalizer.

170. (New) The apparatus of claim 169, further comprising a media access controller coupled to said decoder circuit.

171. (New) The apparatus of claim 167, wherein said digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer.

172. (New) The apparatus of claim 167, wherein said timing recovery circuit shifts the phase of the clock signals in accordance with a product of a plurality of signal samples.

173. (New) The apparatus of claim 167, wherein the twisted wires further carry analog timing signals, wherein the analog to digital converter is arranged to convert the analog timing signal to corresponding timing digital signals in response to the clock signals, and wherein the timing recovery circuit is arranged to shift the phase of the clock signals in response to the timing digital signals.

174. (New) The apparatus of claim 173 wherein the timing recovery circuit is arranged to shift the phase of the clock signals in response to both the timing digital signals and the information digital signals.

175. (New) The apparatus of claim 167, wherein the plurality of analog levels defining information signals comprises more than two analog levels.

176. (New) A method for recovering a plurality of analog levels defining information signals transmitted on at least one pair of twisted wires comprising:

generating clock signals having a phase;

converting the plurality of analog levels to corresponding digital information signals in response to the clock signals;

shifting the phase of the clock signals so that the time at which the converting occurs is adjusted; and

identifying one of the digital information signals with a level corresponding most closely to one of the plurality of analog levels defining information signals.

177. (New) The method of claim 176, wherein said shifting comprises shifting the phase of the clock signals in accordance with a product of a plurality of signal samples.

178. (New) The method of claim 176 and further comprising decoding the identified digital information signals.

179. (New) The method of claim 176, and further comprising a method of recovering analog timing signals wherein the converting also comprises converting the analog timing signals to corresponding timing digital signals in response to the clock signals, and wherein the shifting comprises shifting the phase of the clock signals in response to the timing digital signals.

180. (New) The method of claim 179 wherein the shifting comprises shifting the phase of the clock signals in response to both the timing digital signals and the information digital signals.

181. (New) The method of claim 176, wherein the plurality of analog levels defining information signals comprises more than two analog levels.

182. (New) The apparatus of claim 145, wherein the twisted wires further carry analog timing signals, wherein the analog to digital converter is arranged to convert the analog riming signals to corresponding timing digital signals in response to the clock signals, and wherein timing recovery circuit is arranged to regulate the rate of the clock signals in response to the timing digital signals.

183. (New) The apparatus of claim 182 wherein the timing recovery circuit is arranged to regulate the rate of the clock signals in response to both the timing digital signals and the information digital signals.

184. (New) The apparatus of claim 145 wherein the plurality of analog levels defining information signals comprises more than two analog levels.

185. (New) The method of claim 163, and further comprising a method of recovering analog timing signals wherein the converting also comprises converting the analog timing signals to corresponding timing digital signals at the particular rate, and wherein the regulating comprises regulating the particular rate in response to the timing digital signals.

186. (New) The method of claim 185 wherein the regulating comprises regulating the particular rate in response to both the timing digital signals and the information digital signals.

187. (New) The method of claim 163 wherein the plurality of analog levels defining information signals comprises more than two analog levels.

188. (New) An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal, comprising:

an analog to digital converter for digitally converting the multi-level signal at a particular rate;

a timing recovery circuit for regulating the particular rate at which said analog to digital converter converts the multi-level signal in accordance with a product of a plurality of peak signal samples; and,

a digital adaptive equalizer for receiving the digitally converted multi-level signal and identifying one of a plurality of levels.

189. (New) An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal transmitted at a transmission rate of at least 25 megasymbols per second, comprising:

an analog to digital converter that is responsive to the multi-level signal transmitted at the transmission rate of at least 25 megasymbols per second;

a clock recovery circuit coupled to said analog to digital converter that regulates the particular rate in accordance with a product of a plurality of peak signal samples; and,

a digital adaptive equalizer coupled to said analog to digital converter.

190. (New) An apparatus that is adapted to be coupled to at least one pair of twisted wires that carry a multi-level signal, comprising:

an analog to digital converter operating at a particular rate;

a clock recovery circuit coupled to said analog to digital converter that regulates the particular rate in accordance with a product of a plurality of peak signal samples; and,

a digital adaptive equalizer coupled to said analog to digital converter.

191. (New) A method for recovering a multi-level signal transmitted on at least one pair of twisted wires, comprising:

converting the multi-level signal to a digital signal at a particular rate;

regulating the particular rate of conversion in accordance with a product of a plurality of peak signal samples;

equalizing the digital signal; and,

identifying one of a plurality of levels based on the digital signal.

192. (New) Apparatus adapted to be coupled to at least a twisted first wire pair enabling receipt of at least first, second and third discrete analog signal levels with different amplitudes representing information, a twisted second wire pair enabling

receipt of at least fourth, fifth and sixth discrete analog signal levels with different amplitudes representing information and a twisted third wire pair enabling receipt of at least seventh, eighth and ninth discrete analog signal levels with different amplitudes representing information, the analog signal levels being received one discrete signal level at a time, the apparatus comprising:

an analog to digital converter arranged to convert the first discrete analog signal level to a corresponding digital first information signal, to convert the second discrete analog signal level to a corresponding digital second information signal, to convert the third discrete analog signal level to a corresponding digital third information signal, to convert the fourth analog signal level to a corresponding digital fourth information signal, to convert the fifth discrete analog signal level to a corresponding digital fifth information signal, to convert the sixth discrete analog signal level to a corresponding digital sixth information signal, to convert the seventh discrete analog signal level to a corresponding digital seventh information signal, to convert the eighth discrete analog signal level to a corresponding digital eighth information signal and to convert the ninth discrete analog signal level to a corresponding digital ninth information signal; and

circuitry arranged to individually identify each of the first, second, third, fourth, fifth, sixth, seventh, eighth and ninth discrete analog signal levels, to shift in time the first information signal relative to the first discrete analog signal level, to shift in time the second information signal relative to the second discrete analog signal level, to shift in time the third information signal relative to the third discrete analog signal level, to shift in time the fourth information signal relative to the fourth discrete analog signal level, to shift in time the fifth information signal relative to the fifth discrete analog signal level, to

shift in time the sixth information signal relative to the sixth discrete analog signal level, to shift in time the seventh information signal relative to the seventh discrete analog signal level, to shift in time the eighth information signal relative to the eighth discrete analog signal level and to shift in time the ninth information signal relative to the ninth discrete analog signal level.

193. (New) The apparatus of claim 192 wherein the analog to digital converter is arranged to convert the discrete analog signals levels to corresponding digital information signals at a particular rate and wherein the circuitry comprises a timing recovery circuit arranged to regulate the particular rate at which said analog to digital converter converts the discrete analog signal levels.

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194. (New) The apparatus of claim 193 wherein the circuitry comprises a digital adaptive equalizer arranged to identify the discrete analog signal level being received on each of the wire pairs.

195. (New) The apparatus of claim 194 and further comprising an automatic gain control circuit coupled to the analog to digital converter.

196. (New) The apparatus of claim 194 and further comprising a decoder circuit coupled to the digital adaptive equalizer.

197. (New) The apparatus of claim 196 and further comprising a media access controller coupled to said decoder circuit.

198. (New) The apparatus of claim 194 wherein the digital adaptive equalizer includes a feedforward equalizer, a data slicer and a decision feedback equalizer.

199. (New) The apparatus of claim 194 wherein said timing recovery circuit regulates the particular rate in accordance with a product of a plurality of signal samples.

200. (New) The apparatus of claim 192 and further comprising a clock arranged to generate clock signals having a phase and wherein the analog to digital converter is arranged to convert the discrete analog signal levels to the corresponding digital information digital signals in response to the clock signals and wherein the circuitry is arranged to shift the phase of the clock signals so that the time at which the analog to digital converter samples the discrete analog signal levels is adjusted.

201. (New) The apparatus of claim 200 wherein the circuitry shifts the phase of the clock signals in accordance with a product of a plurality of signal samples.

202. (New) The apparatus of claim 200 where each of the wire pairs also enables receipt of timing discrete analog signal levels, wherein the analog to digital converter is arranged to convert the timing discrete analog signal levels to corresponding timing digital signals in response to the clock signals, and wherein the circuitry is arranged to shift the phase of the clock signals in response to the timing digital signals.

203. (New) The apparatus of claim 202 wherein the circuitry is arranged to shift the phase of the clock signals in response to both the timing digital signals and the information digital signals.

204. (New) In apparatus adapted to be coupled to at least a twisted first wire pair enabling receipt of at least first, second and third discrete analog signal levels with different amplitudes representing information, a twisted second wire pair enabling

receipt of at least fourth, fifth and sixth discrete analog signal levels with different amplitudes representing information and a twisted third wire pair enabling receipt of at least seventh, eighth and ninth discrete analog signal levels with different amplitudes representing information, the analog signal levels being received one discrete signal level at a time, a method of processing the received discrete analog signal levels comprising:

converting the first discrete analog signal level to a corresponding digital first information signal;

converting the second discrete analog signal level to a corresponding digital second information signal;

converting the third discrete analog signal level to a corresponding digital third information signal;

converting the fourth discrete analog signal level to a corresponding digital fourth information signal;

converting the fifth discrete analog signal level to a corresponding digital fifth information signal;

converting the sixth discrete analog signal level to a corresponding digital sixth information signal;

converting the seventh discrete analog signal level to a corresponding digital seventh information signal;

converting the eighth discrete analog signal level to a corresponding digital eighth information signal;

converting the ninth discrete analog signal level to a corresponding digital ninth information signal;

individually identifying each of the first, second, third, fourth, fifth, sixth, seventh, eighth and ninth discrete analog signal levels;

shifting in time the first information signal relative to the first discrete analog signal level;

shifting in time the second information signal relative to the second discrete analog signal level;

shifting in time the third information signal relative to the third discrete analog signal level;

shifting in time the fourth information signal relative to the fourth discrete analog signal level;

shifting in time the fifth information signal relative to the fifth discrete analog signal level;

shifting in time the sixth information signal relative to the sixth discrete analog signal level;

shifting in time the seventh information signal relative to the seventh discrete analog signal level;

shifting in time the eighth information signal relative to the eighth discrete analog signal level; and

shifting in time the ninth information signal relative to the ninth discrete analog signal level.

205. (New) The method of claim 204 wherein each of the converting steps comprises converting one of the discrete analog signals levels to a corresponding one of the information signals at a particular rate and further comprising regulating the particular rate.

206. (New) The method of claim 205 wherein said regulating comprises regulating the particular rate in accordance with a product of a plurality of signal samples.

207. (New) The method of claim 204 and further comprising controlling the gain of the each of the received discrete analog signal levels.

208. (New) The method of claim 204 and further comprising decoding each of the digital information signals.

209. (New) The method of claim 204 and further comprising controlling media access.

210. (New) The method of claim 204 and further comprising generating clock signals having a phase and wherein each of the converting steps comprises converting one of the discrete analog signal levels to one of the corresponding digital information signals in response to the clock signals and wherein each of the shifting steps comprises shifting the phase of the clock signals so that the time at which the converting occurs is adjusted.

211. (New) The method of claim 210 wherein the shifting comprises shifting the phase of the clock signals in accordance with a product of a plurality of signal samples.

212. (New) The method of claim 210 wherein each of the wire pairs enables receipt of timing discrete analog signal levels, wherein the converting further comprises

converting the timing discrete analog signal levels to corresponding timing digital signals in response to the clock signals, and wherein the shifting further comprises shifting the phase of the clock signals in response to the timing digital signals.

213. (New) The method of claim 212 wherein the shifting comprises shifting the phase of the clock signals in response to both the timing digital signals and the digital information signals.

Please add the following claims:

214. (New) A communication system for decoding signals having three or more analog signal levels to represent information transmitted by a first computer over a plurality of pairs of twisted wires to a second computer, said communication system including a transceiver comprising:

a plurality of receivers and transmitters operatively coupled to respective ones of said plurality of said pairs of twisted wires, wherein each of said plurality of receivers comprises:

an analog to digital converter;

an automatic gain control circuit; and

a digital adaptive equalizer, said equalizer further comprising a feed forward equalizer, a decision feedback equalizer, and a data slicer;

wherein each of said analog to digital converters sampling said analog signal at a sampling rate, each of said automatic gain control circuits receiving said analog signal from one of said pairs of twisted wires and providing gain control at the input to a respective one of said analog to digital converters, and each of said equalizers producing recovered digital data from said sampled analog signal provided at the input

of said equalizer; and

wherein said transceiver also includes a plurality of transmitters that simultaneously transmit three or more analog signal levels to said first computer over said plurality of pairs of twisted wires.

215. (New) The system of claim 214, wherein said transceiver combines said recovered data from each of said digital adaptive equalizers into a single recovered digital data stream.

216. (New) The system of claim 215, wherein said single recovered data stream is Ethernet data.

217. (New) The system of claim 214, wherein said communication system is an Ethernet system.

218. (New) The system of claim 214, wherein the digital data is Ethernet data with a data rate of at least 100 Mbps.

219. (New) The system of claim 214, wherein each of said equalizer includes an adder that sums the output of respective ones of said decision feedback equalizers and said feed forward equalizers.

220. (New) The system of claim 219, wherein the digital data is Ethernet data.